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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/535,233	03/24/2000	Masaya Kadono	SEL 171	1670

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EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/535,233	KADONO ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☒ Claim(s) *37-42* is/are allowed.

6)☒ Claim(s) *11-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Examiner's Comments

It appears that the Office Action mailed January 10, 2006 did not address the limitations of the amended claims of the RCE filed October 10, 2005.

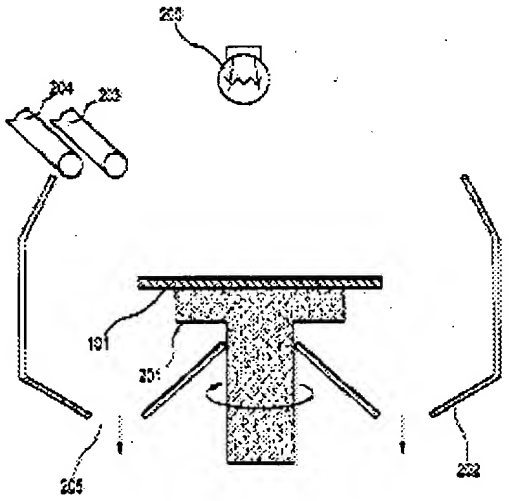
1.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 11-18, 23-32 and 34-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Konuma, U.S. Patent 6,127,279.



3. Konuma discloses a semiconductor process as claimed.

Pertaining to claim 11, Konuma teaches a method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film over a substrate having an insulating surface;

forming a patterned resist mask over said semiconductor film (not shown, however please note in column 6, lines 62-68, Konuma teaches a fabrication technique of forming a silicon oxide film 101 by sputtering, an amorphous silicon film, i.e., semiconductor film is then formed to a thickness of 500 angstroms, an island like film is only formed after patterning as disclosed in column 7, lines8-14);

patterning said semiconductor film to form at least one semiconductor island;

spinning the substrate after removing the patterned resist mask (after development of the resist mask, please note that portions of the resist are removed i.e., undeveloped portions);

applying an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the semiconductor island by the step of applying the etching solution; and then

forming a gate insulating film in contact with said semiconductor film from the surface of which the contaminating impurity has been removed.

4. Pertaining to claim 12, Konuma teaches a method according to claim 11, wherein the contaminating impurity is at least one element selected from periodic table group 1 elements or periodic table group 2 elements (the Examiner takes the position that it is well known to remove contaminants with a fluoric acid solution which was previously discussed by Kern).

5. Pertaining to claim 13, Konuma teaches a method according to claim 11, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg. Ca and Ba .

6. Pertaining to claim 14, Konuma teaches a method according to claim 11, wherein the contaminating impurity is removed by an acidic solution containing fluorine .

7. Pertaining to claim 15, Konuma teaches a method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film over a substrate having an insulating surface **702**;

forming a patterned resist mask over said semiconductor film;

patterning said semiconductor film to form at least one semiconductor island;

removing the patterned resist mask located over said semiconductor island;

spinning the substrate after removing the patterned resist mask;

applying an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the semiconductor island by the step of applying the etching solution;

forming a gate insulating film over said semiconductor island after the contaminating impurities are removed from the surface of the semiconductor island;

spinning the substrate having the gate insulating film;

applying an etching solution to a surface of said gate insulating film and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the gate insulating film by the step of applying the etching solution; and then

forming a gate electrode over said gate insulating film after the contaminating impurities are removed from the surface of the gate insulating film.

8. Pertaining to claim 16, Konuma teaches a method according to claim 15, wherein said etching solution is selected from the group consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF, hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride (NH_4HF_2) and ammonium fluoride (NH_4F).

9. Pertaining to claim 17, Konuma teaches a method according to claim 15, wherein the contaminating impurity is at least one element selected from periodic table group I elements or periodic table group II elements (please see the rejection of claim 13 above).

Pertaining to claim 18, Konuma teaches a method according to claim 15, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg, Ca, and Ba.

10. Pertaining to claims 23 and 27, Konuma teaches a method of manufacturing a semiconductor device, comprising steps of:

forming a gate wiring over a substrate having an insulating surface;

spinning the substrate;

applying an etching solution to surfaces of said substrate and said gate wiring and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the wiring and the insulating surface by the step of applying the etching solution; and then forming a gate insulating film and a semiconductor film over said gate wiring after the contaminating impurities are removed from the surfaces (the Examiner takes the position that

since Konuma teaches the fabrication of various semiconductor devices, the wiring layer is inherent).

11. Pertaining to claims 24, 28 and 31, Konuma teaches a method according to claims 11, 23 and 27, wherein said etching solution is selected from the group consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF, hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride (NH_4HF_2) and ammonium fluoride (NH_4F).

12. Pertaining to claim 25 and 29, Konuma teaches a method according to claims 23 and 27, wherein the contaminating impurity is at least one element selected from periodic table group I elements or periodic table group II elements.

13. Pertaining to claims 26 and 30, Konuma teaches a method according to claims 23 and 27, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg, Ca, and Ba..

14. Pertaining to claims 33, 34 and 35, Konuma teaches a method according to claims 15, 23 and 27, wherein the contaminating impurity is removed by an acidic solution containing fluorine (see the rejection of claim 12 above).

15. Claims 19-22 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Chiyou et al., Patent Abstracts of Japan 11-016866.

Chiyou discloses a semiconductor process as claimed.

16. Pertaining to claim 19, Chiyou teaches a method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film **3** formed over a substrate **1** having an insulating surface **2**;

crystallizing said semiconductor film [0052];

forming a patterned resist mask over said crystallized semiconductor film (please note that it is well known to pattern transistor with a resist prior to etching as disclosed by Chiyou);

patterning the crystallized semiconductor film to form at least one semiconductor island (transistors on a substrate will inherently form islands) over said substrate;

removing the patterned resist mask located over said semiconductor island (a necessary requirement to make functional devices);

spinning the substrate [0051] after removing the patterned resist mask (unwanted portions of the resist mask are removed);

forming at least one semiconductor island over said substrate by patterning the crystallized semiconductor film [see Drawing 3];

applying an etching solution to a surface of said semiconductor film and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the semiconductor island; and then

forming a gate insulating film over said semiconductor island after the contaminating impurities are removed from the surfaces by the step of applying the etching solution; and

forming a gate electrode over said gate insulating film (please note that since Chiyou teaches DRAM, EPROM, MPU and switching transistor and a liquid crystal display the gate electrode and gate insulating layer is well known to be incorporated in the above devices).

17. Pertaining to claim 20, Chiyou teaches a method according to claim 19, wherein said etching solution is selected from the group consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF), hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride (NH_4HF_4) and ammonium fluoride (NH_4F) (LAL500).

18. Pertaining to claim 21, Chiyou teaches a method according to claim 19, wherein the contaminating impurity is at least one element selected from periodic table group I elements or periodic table group II elements (the Examiner takes the position that it is well known that metal ions from the group I and group II elements of the periodic table as conventional contaminants for the silicon process).

19. Pertaining to claim 22, Chiyou teaches a method according to claim 19, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg, Ca and Ba (the examiner takes the position that the claimed elements are one of the major sources of contaminants).

20. Pertaining to claim 36, Chiyou teaches a method according to claim 19, wherein the step of crystallization is performed by irradiating a laser light [0046].

Allowable Subject Matter

21. Claims 37-42 allowed.

22. The following is an examiner's statement of reasons for allowance: the prior art does not anticipate nor render obviousness as to a second spin etching step.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823